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09/602,422	06/23/2000	Subramanian S. Meiyappan	VLSI-3505	1374

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EXAMINER

WHITMORE, STACY

ART UNIT      PAPER NUMBER

2812

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/602,422

Applicant(s)

MEIYAPPAN ET AL.

Examiner

Stacy A Whitmore

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 June 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 and 6 is/are allowed.
- 6) ☒ Claim(s) 5, 7, 8, 11, 13 and 16-22 is/are rejected.
- 7) ☒ Claim(s) 1-4, 8, 10, 12, 14 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 4-8, 10, 12, 14, and 20, are objected to because of the following informalities:
  - I. In claims 1, 4, 8, and 14, the term "SoC" is not properly described prior to the term being used. The term should be introduced in the claims as system on a chip (SoC) before using just the acronym of the phrase.
  - II. In claim 20, the term "GUI" is not properly described prior to the term being used. The term should be introduced in the claims as graphical user interface (GUI) before using just the acronym of the phrase.
  - III. In claims 5, 7, and 14, the term "IC" should be introduced as integrated circuit (IC) before just using the acronym.
  - IV. In claim 1, line 12, "the term "said parameter application module" refers to "a parameter application module" which appears in the claim after the reference to the "said parameter application module" which should be clarified (e.g., the phrase could be corrected by changing to "a parameter application module").
  - V. In claim 6, line 4, the phrase "the selected circuit blocks" refers to "selection of standardized circuit blocks". The phrase "the selected circuit blocks" should more accurately be phrased "the selected standardized circuit blocks".
  - VI. In claim 7, line 1, "an" should be changed to "a".
  - VII. In claim 8, the phrase "said selected circuit blocks" refers to ""standardized circuit blocks" which should be more accurately be phrased ""said selected standardized circuit blocks".
  - VIII. In claim 10, lines 6 and 8, the phrase "parameterizable command line string" refers to "corresponding string". The phrase "corresponding string" is a "parameterizable command line string" as indicated in the specification on pg. 20, lines

16-18. The phrase "corresponding string" should be changed to more accurate claim language such as "parameterizable command line string".

IX. In claim 12, line 3, the term "circuit block" refers to "circuit block designs" in line 3 of claim 7. The phrase "circuit block" should be more accurately phrased to refer back to "circuit block designs" (e.g. change "circuit block" to "the circuit block designs").

Appropriate correction is required.

*Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 11, 13, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 5 recites the limitation "the circuit blocks" in line 3. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 11 recites the limitation "the circuit block attributes" in line 3. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 13 recites the limitation "the applied parameter information" in line 3. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 15 recites the limitation "each of those components" in line 6. There is insufficient antecedent basis for this limitation in the claim.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 16-19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Blaner, B., et al., "RTL design source management for system-on-a-chip designs".
8. As for claims 16-19, and 21, Blaner taught the invention as claimed, including a system on a chip netlist builder and verification computer method comprising the steps of:
  - receiving system specification information [pg. 149, section 3 - architectural definition phase];
  - reusing standardized circuit block information [pg. 147, see IP cores];
  - performing test bench integration [pg. 152, paragraphs 1-4];
  - determining if a proposed circuit design passes a test [pg. 152, left hand side, verification, and test pass/fail];
  - synthesizing circuit blocks [pg. 150 first paragraph, synthesizable cores]; and
  - creating a top level netlist [pg. 149, first paragraph, "Soft cores from IBM ASICs core library are delivered as technology-dependent VDHL or Verilog netlists", and Logic developed for the customer and chip top-level logic are coded and delivered in VDHL or Verilog form...", this reads as a creation of top level netlist].
9. [claim 17] receiving information associated with custom designed circuit blocks [pg. 148, right-hand side, "Custom logic" section].
10. [claim 18] writing a test [pg. 152, left hand side, first paragraph].
11. [claim 19] facilitating communications from a user regarding circuit block selection and parameterization [pg. 147, section 1, designer selects third-party IP core,

and pg. 148, "third-party core", which shows the Third-party IP core to be parameterizable, and pg. 149, section 3, first paragraph].

12. [claim 21] retrieving appropriate information from storage sources [pg. 149, cores delivered from library, which reads on appropriate information retrieved from a storage source, because the cores in a library (group of computer files) are inherently retrieved from a storage source].

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner et al., "RTL design source management for system-on-chip designs".

As for claim 22, Blaner taught the invention substantially as claimed, including the stem on a chip netlist builder and verification computer method as cited in the rejection claim 16. Blaner further taught generating HDL files for building blocks [pg. 149, left hand side, first paragraph], connections of building blocks, and an external I/O block [pg. 148, fig. 1, and pg 149, right hand side bottom paragraph]. Blaner further taught the functions of design, synthesis, simulation, and verification of the building blocks, and external I/O. However, Blaner did not specifically teach that the HDL files describe connections between the building blocks, or that the HDL files are created for the external I/O. However, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to have HDL files that describe connections between the building blocks, and HDL files that are created for the external I/O because HDL netlist (files) would provide the circuit representations of the connections and external I/O which could then be used to perform the functions that Blaner teaches.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner et al., "RTL design source management for system-on-chip designs" in view of Lawman et al (US Patent 6,118,938).

[note: a present system GUI is defined in the specification on page 5, lines 21-22 to be a user friendly and convenient interface for easy entry and modification of user selections and parameters]

14. As for claim 20, Blaner taught the invention substantially as claimed, including the stem on a chip netlist builder and verification computer method including the system specification information [see as cited in the rejection claim 16]. Blaner did not specifically teach the system specification information is received via a present invention GUI. However, Lawman taught a present system GUI [abstract, fig.'s 4 and 5, and col. 3, lines 6-14]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blaner and Lawman because the use of a GUI would make the input of information easier.

15. Claims 7-8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner et al., "RTL design source management for system-on-chip designs" in view of Lawman et al (US Patent 6,118,938), and Gupte et al. (US Patent 5,903,475).

16. As for claims 7-8, Blaner taught the invention substantially as claimed, including in a computer system, an system on a chip netlist builder and verification computer

method for facilitating creation and modification of IC designs utilizing existing circuit block designs, said method comprising the steps of:

implementing a chip level netlist generation process including core netlist [pg. 149, first paragraph, "Soft cores from IBM ASICs core library are delivered as technology-dependent VHDL or Verilog netlists", and Logic developed for the customer and chip top-level logic are coded and delivered in VHDL or Verilog form...", this reads as a creation of top level netlist]; and verifying a system on a chip design automatically [pg. 152, paragraphs 1-4]

[claim 8] presenting information regarding operations of said SoC netlist builder and verification method to a user [pg. 149, section 3, first, third and fourth paragraphs, ]; and facilitating selection of standardized circuit blocks and parameterization of said selected circuit blocks [Blaner, pg. 147, section 1, designer selects third-party IP core, and pg. 148, "third-party core", which shows the Third-party IP core to be parameterizable, and pg. 149, section 3, first paragraph].

[claim 13] extracting circuit block descriptions from a storage location based upon the applied parameter information [pg. 148, third party core IP section, and pg. 149, unit design phase and chip design phase sections].

Blaner did not specifically teach [claim 7] providing a user friendly interface; performing a parameter application process; and executing an expert system process; [claim 8] assisting easy entry and modification of user selections and parameters; or I/O pin netlists.

Lawman taught [claim 7] providing a user friendly interface; performing a parameter application process, and [claim 8] assisting easy entry and modification of user selections and parameters [abstract, fig.'s 4 and 5, and col. 3, lines 6-14]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blaner and Lawman because Lawman's user friendly interface

allows for the easy entry and modification of user selections and parameters [abstract]. Gupte further taught executing an expert system process [fig.'s 17-19, expert system], and I/O pin netlists [col. 7, lines 36-38]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blaner, Lawman, and Gupte because Gupte's expert system process would have improved Blaner's system in view of Lawman by allowing for the retrieval of HDL code for specific design versions [Gupte, col. 18] which would aid the circuit design process. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Gupte's I/O pin netlists in order to simulate Blaner's system in view of Lawman on a chip which would aid in testing the circuit design [Blaner, pg. 152, left hand side, paragraph 4].

17. Claims 1-4, and 6 are allowable over the prior art of record. Note that claims 1, 4, and 6 have claim objections that need to be addressed before allowance.

18. Claims 5, 11, and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

19. Claims 9-10, 12, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Note that claims 10, 12, and 14 also have claim objections that need to be addressed before allowance

20. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach either singularly or in combination a system of a chip netlist builder and verification computer system having a software modules (expert system module, parameter application module, chip level netlist generation module and verification module which interact and pass information

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between modules as claimed in claim 1. As for claims 9-12, and 14-15, the prior art fails to teach an system on a chip netlist builder and verification computer method for facilitating creation and modification of IC designs utilizing existing circuit block designs wherein an underlying structure list is created and wherein iterations are performed the generate an underlying structure list; initializing a command line string, making an instance specific copy and updating the copy of the string; appending circuit block attributes to other files and adding gate counts to a list of gate counts; generating an internal integration list and using the integration list in the processing of other routines; creating IC core level netlist based on data structures that were populated in other routines; and producing HDL assign statements in accordance with an assignment list and instantiating each component based on the instantiation list.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,311,309	Southgate	testbench, GUI, simulation
6,145,073	Cismas	predefined cores
5,841,663	Sharma	HDL modules
6,102,961	Lee	IP blocks
5,428,791	Andrew	generic user interface and builder modules

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for


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the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy Whitmore  
August 9, 2002

  
PATENT EXAMINER  
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